

September 1998

## Quad 2-Input NOR Gate

### Features

- **Typical Propagation Delay**
  - 6ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$
- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω Transmission Lines

### Description

The CD74AC02 and CD74ACT02 are quad 2-input NOR gates that utilize the Harris Advanced CMOS Logic technology.

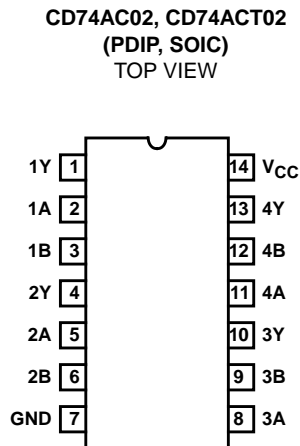
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74AC02E	-55 to 125	14 Ld PDIP	E14.3
CD74ACT02E	-55 to 125	14 Ld PDIP	E14.3
CD74AC02M	-55 to 125	14 Ld SOIC	M14.15
CD74ACT02M	-55 to 125	14 Ld SOIC	M14.15

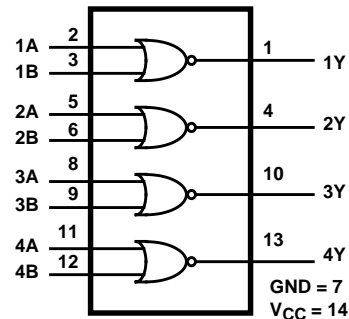
#### NOTES:

- When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
- Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout



### Functional Diagram



#### TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

## CD74AC02, CD74ACT02

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 6V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 50mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 3) .....	$\pm 100mA$

### Thermal Information

Thermal Resistance (Typical, Note 5)	$\theta_{JA}$ (°C/W)
PDIP Package .....	90
SOIC Package .....	175
Maximum Junction Temperature (Plastic Package) .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C

### Operating Conditions

Temperature Range, $T_A$ .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$ (Note 4)	
AC Types .....	1.5V to 5.5V
ACT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Slew Rate, dt/dv	
AC Types, 1.5V to 3V .....	50ns (Max)
AC Types, 3.6V to 5.5V .....	20ns (Max)
ACT Types, 4.5V to 5.5V .....	10ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTES:

14. For up to 4 outputs per device, add  $\pm 25mA$  for each additional output.
15. Unless otherwise specified, all voltages are referenced to ground.
16.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
<b>AC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	1.5	1.2	-	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	2.1	-	V	
				5.5	3.85	-	3.85	-	3.85	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	1.5	-	0.3	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	-	0.9	V	
				5.5	-	1.65	-	1.65	-	1.65	V	
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	1.5	1.4	-	1.4	-	1.4	-	V	
			-0.05	3	2.9	-	2.9	-	2.9	-	V	
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V	
			-4	3	2.58	-	2.48	-	2.4	-	V	
			-24	4.5	3.94	-	3.8	-	3.7	-	V	
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V	
-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V				

## CD74AC02, CD74ACT02

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Quiescent Supply Current SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	4	-	40	-	80	μA
<b>ACT TYPES</b>											
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Quiescent Supply Current SSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	4	-	40	-	80	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

**NOTES:**

17. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
18. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

### ACT Input Load Table

INPUT	UNIT LOAD
All	0.32

NOTE: Unit load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

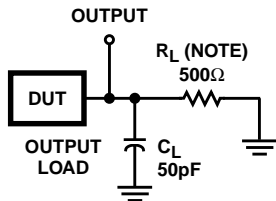
## CD74AC02, CD74ACT02

### Switching Specifications Input $t_r, t_f = 3\text{ns}$ , $C_L = 50\text{pF}$ (Worst Case)

PARAMETER	SYMBOL	$V_{CC}$ (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>AC TYPES</b>									
Propagation Delay, Input to Output	$t_{PLH}, t_{PHL}$	1.5	-	-	131	-	-	144	ns
		3.3 (Note 9)	4.1	-	14.6	4	-	16.1	ns
		5 (Note 10)	3	-	10.4	2.9	-	11.5	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	55	-	-	55	-	pF
<b>ACT TYPES</b>									
Propagation Delay, Input to Output	$t_{PLH}, t_{PHL}$	5 (Note 10)	3.1	-	11.1	3.1	-	12.2	ns
Input Capacitance	$C_I$	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	55	-	-	55	-	pF

**NOTES:**

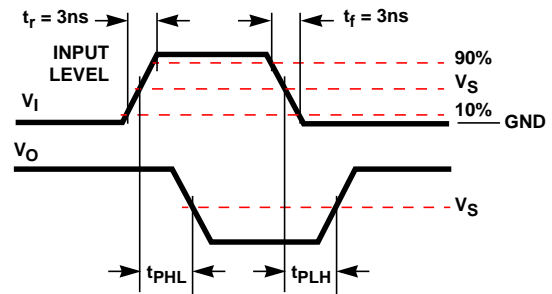
19. Limits tested at 100%.
20. 3.3V Min at 3.6V, Max at 3V.
21. 5V Min at 5.5V, Max at 4.5V.
22.  $C_{PD}$  is used to determine the dynamic power consumption per gate.  
 AC:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$   
 ACT:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.



NOTE: For AC Series Only: When  $V_{CC} = 1.5\text{V}$ ,  $R_L = 1\text{k}\Omega$ .

	CD74AC	CD74ACT
Input Level	$V_{CC}$	3V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

**FIGURE 2. PROPAGATION DELAY TIMES**



**FIGURE 3. PROPAGATION DELAY TIMES**

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